IAR visualSTATE®—state machine design automation for embedded systems

IAR visualSTATE is a set of highly sophisticated and easy-to-use development tools for designing, testing and implementing embedded applications based on statechart diagrams. It provides advanced verification and validation utilities and generates very compact C/C++ code that is 100% consistent with your system design. In addition, the new and revolutionizing integration with IAR Embedded Workbench®, a fully integrated C/C++ compiler and debugger toolset, enables true state machine debugging on hardware---with direct graphical feedback at various levels of detail.

KEY FEATURES

- Completely integrated development environment including graphical designer, test tools, code generator, and documentation tool
- Graphical state machine design based on the Unified Modeling Language (UML) state machine subset
- Formal verification of the design model finds unwanted properties in the design, like dead-ends or unreachable states etc.
- Test and validation tools to ensure at an early stage of design that the application behaves as expected, even before the hardware exists!
- Automatic code generation providing an option between generating very compact table based C/C++ code or readable code 100% compliant with the design
- Automatic documentation generation with comprehensive information
- Tightly integrated with IAR Embedded Workbench, providing smooth interaction between the tools on all levels from file and build management, to target debugging
- Ready-made project examples for various microcontrollers and evaluation boards

BENEFITS

- Stay in the high-level domain, focusing on the state machine design, instead of low level implementation details
- Validate your design against requirements, starting as soon as you begin your design work
- Find potentially hazardous problems in your design with the aid of the formal verificator, instead of finding them in acceptance tests or at customer sites

- Debug complex scenarios in C-SPY with high-level graphical feedback and the possibility to set breakpoints on the state machine level
- Use a smaller target device—thanks to lower RAM and ROM requirements— thus saving on per-unit cost
- Deliver higher quality to market in less time

APPLICATION AREAS

IAR visualSTATE is the perfect tool for managing rising complexity in reactive, state based applications or parts of applications. All problems that are best described as state machines can be designed in visualSTATE, no matter the level of complexity. The test and verification tools guarantee the quality. Examples include:

- Life science applications and medical devices for personal use
- Applications with Man Machine interaction, like media players, household appliances, etc.
- Industrial automation, including building automation
- All kinds of applications where RAM and ROM size is a factor combined with high quality or integrity requirements

GRAPHICAL PROJECT MANAGEMENT

- Fully integrated graphical environment
- Smart Navigator handling projects, systems and various types of files
- Source code control with the built-in visualSTATE Multi-User Management or any system that supports Microsoft
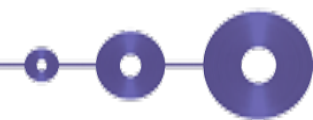
Common Source Code Control (Microsoft SCC API)
- Custom commands for performing specific tasks

STATE-OF-THE-ART DESIGNER
- Graphics-based state machine design tool using the UML subset focusing on control logic expressed as state machines
- Application design by drawing objects, events, actions etc.
- Easy access to all system elements through a tree browser
- Context-sensitive pop-up menus

AUTOMATED SYSTEM ANALYSIS AND TEST
- Advanced formal verification checks the system's logical consistency and identifies a number of potentially hazardous properties of the design, such as
  - Local or system dead-ends
  - Unreachable states or state combinations
  - Force state actions and conflicting transitions
  - Systems with ambiguous behavior etc.
  - Generation of test sequences to bring the system into a problematic state
- Powerful validation for static and dynamic system analysis
  - Interactive simulation to test the functionality of your design, including graphical animation and use of conditional breakpoints
  - Automatic simulation by recording and playing test sequences
  - Automatic analysis of test logs to obtain coverage metrics for the model
  - Playback of test sequences for regression testing
- Comprehensive graphical state machine debugging on the target device via C-SPYLink or RealLink

C-SPYLink– a plug-in solution for the IAR C-SPY Debugger, supporting various hardware debug interfaces, such as J-Link, or a general JTAG probe, NEXUS etc. (the corresponding C-SPY drivers are provided by IAR Embedded Workbench)
- Live monitoring of the complete global state of the state machine system
- Arbitrarily complicated breakpoints on specific events, signals or at state machine level
- Direct graphical feedback with various levels of detail, like current state vector, executed actions, received events etc
- Logging facilities to record the status at the state machine level

- Full-speed execution

RealLink– supporting multiple communication connections, such as RS232, CAN, Ethernet, Bluetooth™, TCP/IP or any other type of communication link

AUTOMATIC C/C++ CODE GENERATION AND DOCUMENTATION
- Generating compact C/C++ code, 100% consistent with your design
- Possibility to exclude design regions from code generation, validation and verification to create variations of the model
- Automatic documentation generation with comprehensive information

INTEGRATION AND COMPATIBILITY
- Easy integration with GUI builder code from almost any tool to create a mock-up of the final application
- Direct connection to an Altia design from the state machine simulator– no need to write any GUI code for prototyping
- Easy integration with any RTOS, but no dependence on any OS services
- The paradigm of parallel state machines can in some situations even remove the need for a simple task-switching OS.
- Tightly integrated with IAR Embedded Workbench, supporting target- and compiler-specific memory attributes and keywords
- Code compatible with any ANSI C compiler with most popular debuggers and emulators

IAR Embedded Workbench®
IAR Embedded Workbench is a set of highly sophisticated and easy-to-use development tools for embedded applications. It integrates the IAR C/C++ Compiler™, assembler, linker, librarian, text editor, project manager, and C-SPY® Debugger in an integrated development environment (IDE). With its advanced optimizing technology, IAR Embedded Workbench generates very efficient and compact code for 8-, 16- and 32-bit microcontrollers. Together with IAR Embedded Workbench, IAR visualSTATE forms a complete set of development tools supporting you through the entire development process.

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