DC Unbalance Tolerance Testing in PSE's

Sifos® Technologies

The PoE Impairment

Much like cable attenuation, alien crosstalk, and impedance mismatches present physical layer impairments to packet traffic on 10/100/1000Base-T links, Power-over-Ethernet (PoE) also has the potential to present significant impairment. Unlike other forms of link impairment however, the assessment of PoE effects on link integrity is extremely challenging to characterize. Furthermore, the mechanisms for PoE impairment involve the combination of disparate components including Power Sourcing Equipment (PSE's), Powered Devices (PD's), cabling, and connectors.

Endpoint PSE's (e.g. Ethernet switches) feed power by sourcing DC current into and returning DC current from transformer center taps. PD's receive power by looping DC current from one (sourcing) transformer center tap to another (returning) center tap. By injecting and extracting DC current from transformer center taps, actual DC current ideally splits evenly between each conductor of each twisted pair and thus appears as common mode current.

DC Unbalance Defined

DC Unbalance Current, $\mathbf{I_{unb}}$, is the difference, on any given twisted pair, between DC current flowing in one conductor and DC current flowing in the other conductor. Therefore, $\mathbf{I_{unb}}$ = 0mA if the current splits evenly between both conductors. DC Unbalance can develop in a PoE connection for any of the following reasons:

Table 1: DC Unbalance Causes

Power Sourcing Equipment	Cabling	Powered Device
Transformer center tap offset	UTP electrical length or resistivity differences between pair conductors	RJ-45 connection resistance differences between conductors
Electrical trace resistance differences between conductors	RJ-45 connection resistance differences between conductors	Electrical trace resistance differences between conductors
RJ-45 connection resistance differences between conductors	Patch panel resistance differences between pair conductors	Transformer center tap offset

Additionally, transient DC Unbalance can develop in *any link*, particularly 100Base-Tx links, as a result of data patterns producing baseline wander. The 100Base-Tx specification allows for up to 16mA of resultant DC Unbalance.

IEEE 802.3at (clause 33.2.7) is written to imply that PSE's must "restrict" maximum DC Unbalance Current, though many of the factors that lead to DC Unbalance are outside the PSE's control. Nonetheless, PSE's should not contribute DC Unbalance beyond the levels shown in Table 2 and therefore, they must be designed to **tolerate** between 26.5 mA (Type-1) and 36.5 mA (Type-2) of DC Unbalance current when combining worst case baseline wander effects with $\mathbf{I_{unb}}$(Max). Similarly, PD's must tolerate the same range of DC Unbalance, again for reasons the PD may have no control over.

Table 2: $\mathbf{I_{unb}}$ Contribution

PSE Type	$\mathbf{I_{unb}}$ (Max)
1 (15.4 Watt)	10.5 mA
2 (30 Watt)	20.5 mA

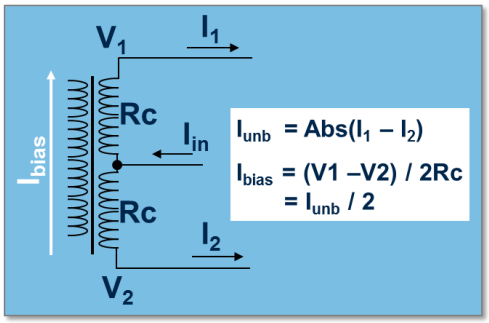

Figure 1: DC Unbalance and $\mathbf{I_{bias}}$

So what does "**tolerate**" really mean? When DC current does not split evenly between each conductor of a twisted pair, the Ethernet transformers at both the PSE and the PD side of the link develop small DC bias currents ($\mathbf{I_{bias}}$ = $\mathbf{I_{unb}}$ / 2) across their primary coils (*see Figure 1*). Much like an electro-magnet or a solenoid, this DC bias produces a magnetic field that compresses, or limits, the magnetic transformer coupling available to AC signals such as the 10/100/1000Base-T signals across the conductor pairs. As $\mathbf{I_{bias}}$ increases, the transformer core starts to saturate resulting in non-linear compression, or distortion, of Ethernet signals as well as attenuated low frequency performance and reduced magnetic coil inductance.

Low frequency performance can also be characterized as pulse droop. The IEEE 802.3at specification added sub-clause 25.4.4a to IEEE 802.3 (100Base-Tx) defining a maximum allowable pulse droop for Ethernet signaling.

Obstacles to Testing DC Unbalance

The simplest way to conceptually generate DC Unbalance on a twisted pair connection would be insert series resistance such that the resistance on each conductor between a PSE and a PD was uneven. This will produce some amount of DC Unbalance, however, the amount of DC Unbalance produced is a function not only of the series resistances but also of the coil DC resistances in each transformer on each side of the link and also a function of PSE voltage. Given this approach, precision ammeters must assess DC current on each conductor while inline power resistors are varied to produce target levels of DC Unbalance.

Once a satisfactory apparatus for creating and assessing magnitude of DC Unbalance is developed, measurements must be performed to assess impact on pulse droop and/or transformer coil inductance. Pulse droop measurements typically require a very high bandwidth scope, calibrated differential probe, and possibly special test mode activation in a transmitting PHY. Coil inductance measurements require a precision, high bandwidth LCR meter with access to pair conductors, tolerance of over 50 VDC, and a disabled PHY transmitter so that Ethernet signaling does not interfere with inductance measurements. Nothing about these types of measurements is very automatable. Consequently, they are seldom performed and only performed on a very low sampling basis.

Automated DC Unbalance Analysis: PVA-3000 + PSA-3000

Sifos Technologies offers a highly unique, plug 'n play, and *fully automated* approach to DC Unbalance tolerance analysis in a power sourcing Ethernet port. This solution, available as part of the PHY Performance Test Suite available for the PVA-3000 PhyView Analyzer, combines one or more PVA-3000 test ports with PowerSync Analyzer (or PowerSync Programmable Load) test ports to assess physical layer signaling response to a range of precisely controlled DC Unbalance conditions.

Test Setup

Figure 2 diagrams the setup required to test a single PSE port for DC Unbalance. This setup requires:

1. A PVA-3000 "TEST" Port
2. A PSA-3000 (or PSL-3000) "TEST" Port
3. A short, preferably Cat6 patch cord from the PVA **TEST** Port to the PSA **OUT** Port
4. A PVA-DCU DC Unbalance Unit
5. A PVA Test Cable from the PSA-3000 **PS***n* Port to the PVA-DCU **PSA** Port*
6. A short, preferably Cat6 patch cord from the PVA-DCU **PSE** port to the PSE port-under-test*

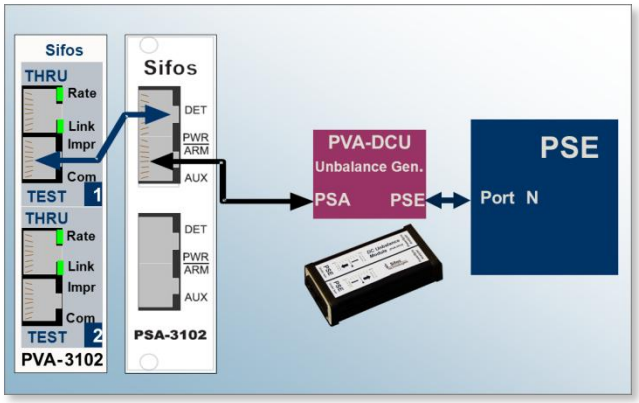

Figure 2: Single Port DC Unbalance Setup

Figure 3: Single Port DC Unbalance Setup, PVA-3002

The PVA-3000 and PSA-3000 (or PSL-3000) test ports may be co-located in a single PSA-3000 chassis, or they may be located in separate instruments. The PVA-3000, PSA-3000, and PSL-3000 instruments are all described within product-specific datasheets published by Sifos Technologies.

Figure 3 presents a DC Unbalance setup using the PVA-3002 Compact PVA and a PSA-3002 Compact PSA.

***Note**: *Items 5 and 6 may be reversed such that the PVA Test Cable connects the PVA-DCU PSE port to the PSE port.*

DC Unbalance Tolerance Testing in PSE's

The PVA-DCU

The **PVA-DCU** (*see Figure 4*) is a small box from Sifos Technologies that works together with the PSA-3000 test port to apply controlled levels of DC Unbalance to a powered PSE port while also biasing the DC Unbalance current so that the PSE experiences greater DC unbalance than the PSA-3000 (or PSL-3000) test port experiences.

Figure 4: PVA-zDCU

The PVA-DCU provides two channels, each of which will create DC Unbalance when ALT-A, ALT-B, or both ALT-A and ALT-B pairsets are providing power from the PSE. One channel unbalances load current from the PSE to the PSA/PSL test port in a positive, or "forward", direction while the other channel unbalances load current in a negative, or "reverse", direction. Generally, DC Unbalance Testing should be run with both positive and negative unbalancing polarities to fully assess PSE tolerance of DC Unbalance.

Table 3: **PVA-DCU** Specifications

Parameter	Value
Forward Channel: ALT-A PSE	Pin 2 > Pin 1, Pin 6 > Pin 3
Reverse Channel: ALT-A PSE	Pin 1 > Pin 2, Pin 3 > Pin 6
Forward Channel: ALT-B PSE	Pin 4 > Pin 5, Pin 7 > Pin 8
Reverse Channel: ALT-B PSE	Pin 5 > Pin 6, Pin 8 > Pin 7
Forward Channel: 4-Pair PSE	Pin 2 > Pin 1, Pin 6 > Pin 3 Pin 4 > Pin 5, Pin 7 > Pin 8
Reverse Channel: 4-Pair PSE	Pin 1 > Pin 2, Pin 3 > Pin 6 Pin 5 > Pin 6, Pin 8 > Pin 7
Unpowered DC Unbalance	0 mA
DC Unbalance (PSA zero load)	22 mA
PSE Load (PSA zero load)	22 mA
DC Unbalance (PSA 350mA load)	76.6 mA
PSE Load (PSA 350mA load)	372 mA

Prior to PSE power-up, PVA-DCU channels are invisible to PD detection and classification processes. This allows the PSA-3000 test port to emulate PD signatures and induce the power-up. When the PSE applies power, the PVA-DCU automatically generates 22mA of DC Unbalance current that will be experienced by the PSE port. Then, as the PSA-3000 test port draws increasing levels of load current, DC Unbalance current will increase linearly from the initial 22mA at a rate of 16% of PSA (or PSL) load current.

Figure 5 depicts a setup to test 2 PSE ports using a PVA-DCU.

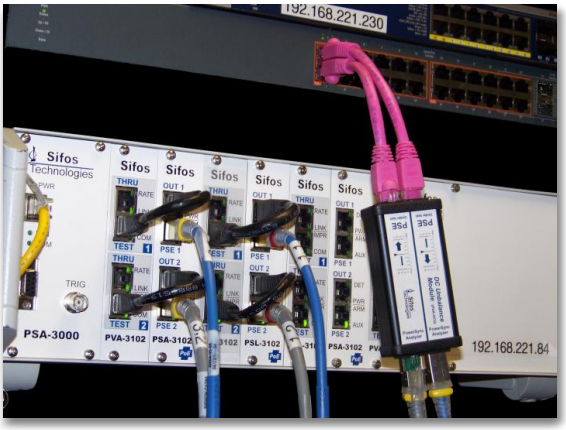

Figure 5: 4-Port DC Unbalance Setup

PVA-3000 Measurements

The PVA-3000 performs physical layer measurements of 10/100/1000Base-T interfaces. Two of those measurements are very relevant to DC Unbalance testing:

- **SNR**: Signal-Noise Ratio (SNR) is an indication of the magnitude of uncorrectable or residual distortion in a 100Base-Tx or 1000Base-T transmitted signal. Ethernet magnetics operating in saturation will compress signals producing non-linear and non-correctable distortion. SNR is reported in dB on a per-pair basis.
- **Low Frequency PSD**: Power Spectral Distortion (PSD) is a measurement of the deviation in transmitted signal power spectrum from a nominally compliant power spectrum for 100Base-Tx and/or 1000Base-T. The DC Unbalance test reports PSD at 50KHz to capture low frequency response while also computing an estimated pulse droop using several low frequency spectral points. PSD is reported in dB on a per-pair basis and Droop is reported in percent on a per-pair basis.

PVA measurements are performed using the **OUT** port of the PSA-3000 (or PSL-3000). This port is DC de-coupled from the PSA **PS***n* port while offering a very low impedance coupling at all frequencies above 10 KHz.

During DC Unbalance testing, the PVA self-calibrates to the PSE port prior to DC power-up in order to compensate for all of the patch cables, the PVA-DCU, and the PSA Test Port coupling. This means that the **SNR** and **Low Frequency PSD** measurements performed are all normalized to the unpowered state of the PSE port. As such, both measurements are a direct indication of the impact of DC Unbalance at the PSE port and do not require any special calibrations.

DC Unbalance Standard Report

When the DC Unbalance test application is run, it will automatically assess PSE characteristics including ALT pairs and PoE polarity as well as support for 100Base-Tx and 1000Base-T. The fully automated testing will then produce a graphical spreadsheet report characterizing the PSE port response to varying levels of DC Unbalance (*see Figure 6*).

The report header displays the instrument and test port resources utilized in the test, the time and date of testing, and any user-described PSE type and port information.

The top graph plots SNR (dB) versus DC Unbalance current. SNR is an indirect indication of bit error probability in a hypothetical receiver. Generally, increased DC Unbalance will decrease SNR. This is heavily a function of quality of magnetics utilized in the PSE.

Plots are provided for 100Base-Tx operating both in MDI (dashed orange) and MDI-X (dashed green) configurations and for 1000Base-T where pair 1 is solid blue, pair 2 is solid orange, pair 3 is solid green, and pair 4 is solid brown.

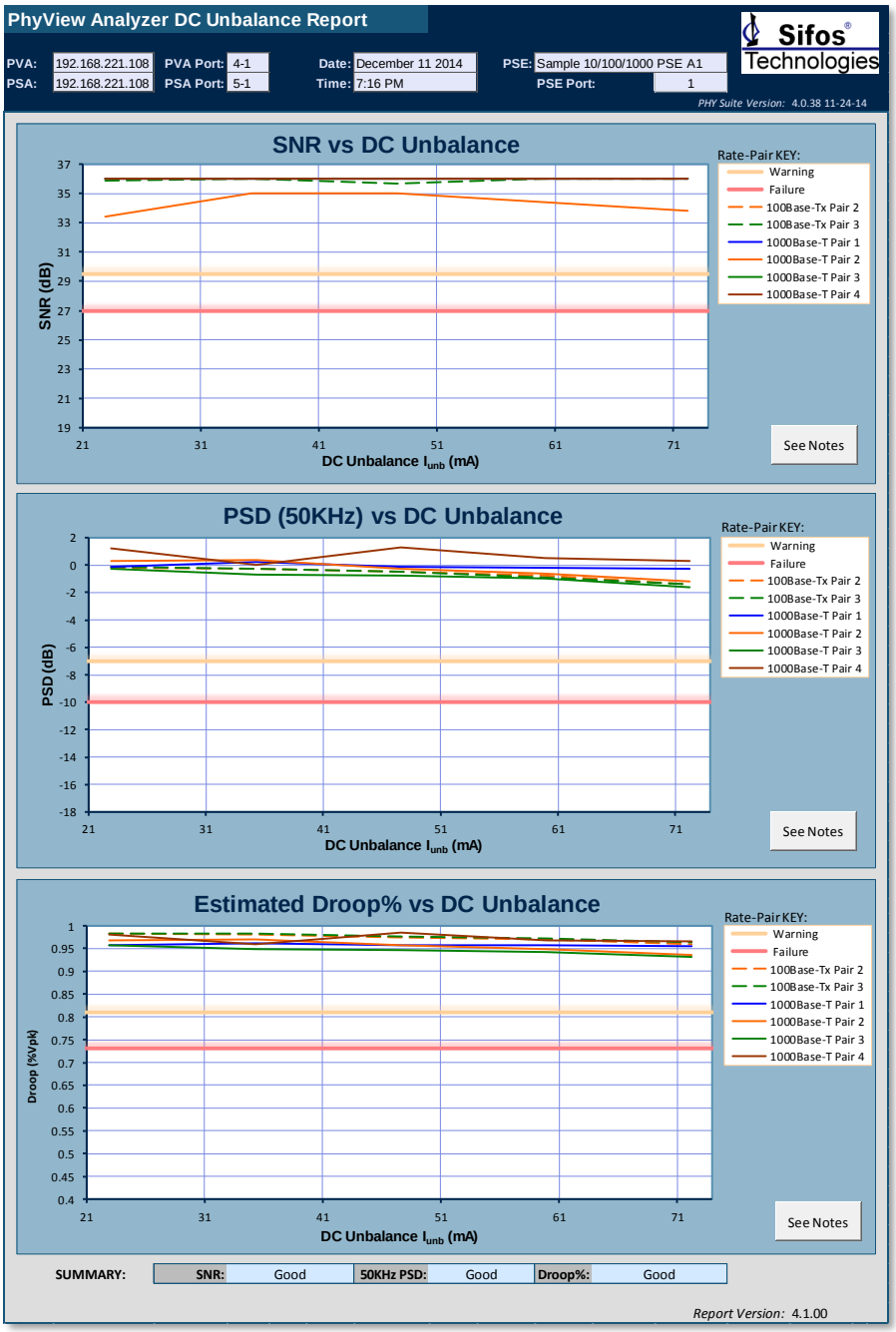

Figure 6: DC Unbalance Standard Report

The middle graph plots 50 KHz Power Spectral Distortion (dB) versus DC Unbalance Current and the lower graph plots Estimated Pulse Droop (%) versus DC Unbalance Current.

In this particular report, a Type-2 (30 Watt) PSE was tested over the range of 22 mA to 72 mA of DC Unbalance Current. It is clear from the plots that the PSE uses ALT-A pairs (2 and 3) for PoE delivery since they show degraded performance as a function of DC Unbalance while the traditional "spare pairs" (1 and 4) are totally unaffected. Overall, this particular PSE port performs very well in response to DC Unbalance, as reported by the indicators at the bottom of the report.

Each graph also presents limit lines for "warning" (yellow) and "problem" (red) performance. These are general guidelines and are not representative of any particular specification.

Figure 7 shows a PSE port that did not perform as well as the PSE port in *Figure 6*. This is also a 30 Watt capable (Type-2, ALT-A) PSE that degrades noticeably at 50 mA of DC Unbalance. It is worth noting that different ports in a multi-port PSE may have wide spreads in DC Unbalance Tolerance performance.

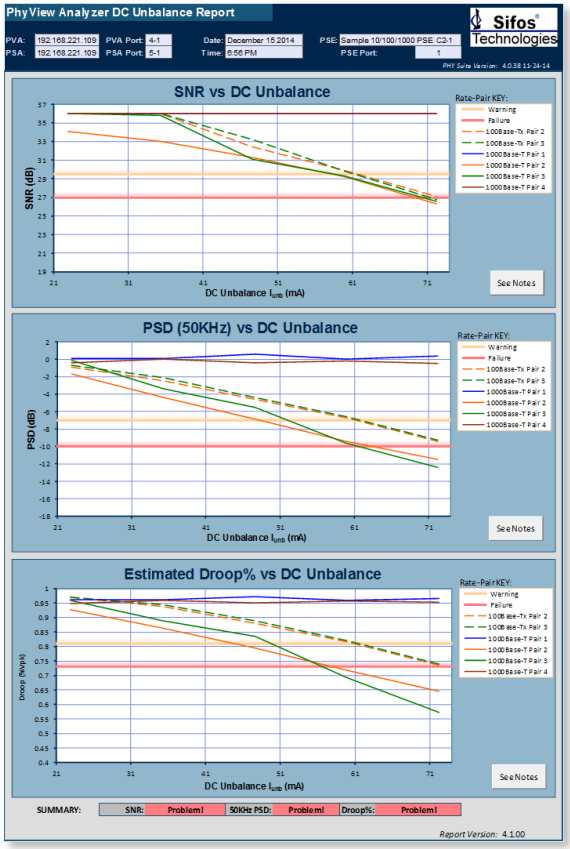

Figure 7: DC Unbalance – Problem PSE Port

The DC Unbalance Application

To run the DC Unbalance application for the PhyView Analyzer, the PVA-3000 must be enabled for the **PHY Performance Test Suite***, a license key enabled feature. If testing is to be performed on a Type-2 PSE that utilizes PoE LLDP protocol for power management, then the PSA-3000 or PSL-3000 instrument must be enabled for **LLDP**, another license key enabled feature. Both the PVA-3000 and PSA-3000/PSL-3000 may reside in a single PSA-3000 chassis.

The DC Unbalance application is available from **PVA Interactive** and from **PowerShell PSA** software, both provided with the PhyView Analyzer. From PVA Interactive, the application is accessed from the **PHY Tests** menu tab (*see Figure 8*) under the **PHY & PoE Tests** sub-menu. Within this menu, users specify the IP address and Test Port of the PSA-3000 (or PSL-3000), the PSE Type as **Type-1** (15.4 watt), **Type-2 PHY** (30 Watt, 2-Event), or **Type-2 LLDP** (30 Watt, LLDP). The check box **Plot Outputs** produces the standard spreadsheet report (*see Figures 6 and 7*) and the DUT Type is optionally specified in the DUT Type entry box above the sub-menu. The slider control **Max Unbalance** is used to specify the largest DC Unbalance current to be generated during testing. For Type-1 PSE's, the maximum supported is **50mA** while for Type-2 PSE's, the largest value supported is **80mA**. The test is run using the currently selected PVA Test Port when **Run Test** is pressed.

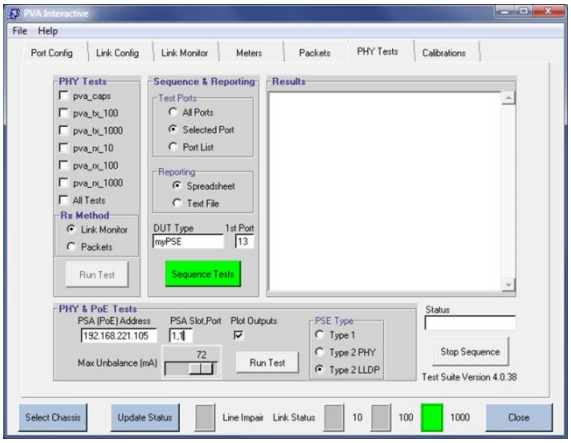

Figure 8: PSA Interactive Software

Figure 9 presents a short PowerShell PSA test script that will sequence testing on 4 PSE ports using a setup similar to that of *Figure 5*. For a gigabit Ethernet PSE, this testing would take about 20 minutes per port tested to complete and will produce four standard reports.

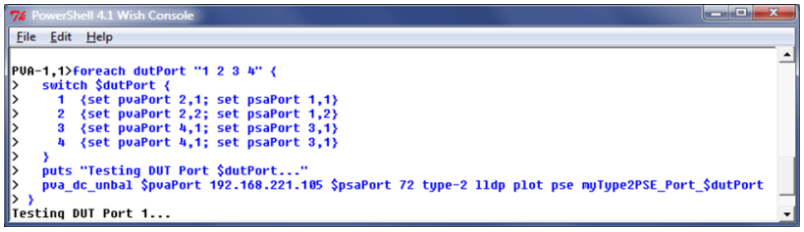

Figure 9: PowerShell PSA Software

* *See Sifos datasheet* **PHY Performance Test Suite Product Overview.pdf** *for further information*.